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IR-1821 (2-2831)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of	New York, New York
Kyle Spring et al.	Date: June 7, 2005
Serial No.: 10/083,060	Group Art Unit: 2814
Filed: February 26, 2002	Examiner: S.H. Rao

For: DEPLETION IMPLANT FOR POWER MOSFET

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. §1.192

Sir:

This appeal is from the Examiner's final rejection of this application dated January 11, 2005.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is:

International Rectifier Corporation

II. RELATED APPEALS AND INTERFERENCES

The applicants, the assignee and the undersigned attorneys are not aware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 11 to 18 are pending and on appeal herein.

Claims 1-10 have previously been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a vertical conduction type power MOSFET of the lateral channel variety.

As is well known, a lateral channel power MOSFET includes a drift region of a first conductivity, a plurality of spaced channel regions (sometimes referred to as base regions or body regions) of a second conductivity formed in the drift region, and source regions of the first conductivity each formed in a respective channel region. Each source region is spaced and isolated from the drift region by a portion of the channel region. In order to enable the electrical connection between a source region and the drift region a gate structure is formed over at least a portion of the channel region residing between the source region and the drift region. As is well known, by application of a minimum voltage (referred to as threshold voltage) to the gate electrode of the gate structure, the conductivity of the portion of channel region residing between the source region and the drift region is changed to that of the source region and the drift region. This process is called inversion, and the region which is changed in conductivity is referred to as the channel.

It is a characteristic of lateral channel devices to have horizontally oriented gate structures in that the channel is horizontally oriented.

Due to the fact that the channel region is of a different conductivity from the drift region, the channel region and the drift region form a PN junction. As is well know, under reverse voltage conditions a depletion region is formed between the channel region and the drift region.

This depletion region advances toward the source, and if there is insufficient charge in the channel region, it reaches the source before avalanche breakdown occurs. This undesirable occurrence is commonly referred to as punch through.

In a low voltage VDMOS device (Vertical Conduction Double Diffused MOS), this premature punch-through is normally prevented by using a higher channel dose and/or a deeper channel drive than might be otherwise required for a given avalanche breakdown value.

However, the higher channel dose results in a correspondingly higher threshold voltage, while a deeper channel drive increases channel length and thus channel resistance. The deeper channel drive also increases the depth of the region between adjacent channel regions (sometimes referred to as JFET region), thus reducing the optimum utilization of the epitaxial silicon in which the drift region is formed.

The present invention is directed at a process for manufacturing a MOSFET in which punch-through is prevented without increasing the threshold voltage of the device or the depth of the channel region. See Fig. 2 of the specification.

According to the invention, a depletion implant is formed in the top surface of the epitaxial silicon for a low voltage lateral channel MOSFET prior to the formation of the channel and source regions.

As a result, there is no need for forming a deep channel region. Thus, the lengthening of the channel is avoided, whereby the increasing of the resistance of the device is avoided. Furthermore, the present technique avoids increasing the threshold voltage. See Fig. 2.

Claim 11, therefore, calls for the following combination:

11. (Currently Amended) A process for manufacturing a planar power semiconductor device comprising:

providing a semiconductor die including an epitaxially grown silicon layer of a first conductivity formed over a substrate;

designating an active area, said active area being a portion of said epitaxially grown silicon layer in which channel regions are formed;

implanting dopants of a second conductivity in all of said active area of said epitaxially grown silicon layer;

forming a plurality of spaced channel regions of said second conductivity in said active area of said epitaxially grown silicon layer, each channel region being spaced from another channel region by a first conductivity region in said epitaxially grown silicon layer;

forming a source region of said first conductivity in each of said channel regions, each source region being less wide and less deep than a channel region in which it is formed; and

forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each channel region.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 11-18 are obvious under 35 U.S.C. §103(a) over Hshieh et al. (Hshieh), U.S. Patent No. 5,907,776 in view of Kumagai et al., U.S. Patent No. 5,477,077 (Kumagai) or in view of Baliga, U.S. Patent No. 4,969,028.

VII. ARGUMENT

Hshieh shows a trench type power MOSFET and discloses a method for making the same.

Referring to Fig. 3, the device shown by Hshieh includes a region of reduced charge adjacent the junction between a source region 48 and body region 50 thereof. As a result, the threshold voltage of the device shown by Hshieh is improved, however, the punch through tolerance of the device is not affected because "the reduction in charge is remote from the origin of the depletion layer which is located at the boundary between the body region and the epitaxial layer." Col. 3, lines 55-65. Thus, Hshieh makes it clear that charge variation that it proposes does not reach the junction between the body region 50 and epitaxial layer 52 (drift region of the device).

Fig. 5 graphically illustrates the concept that is proposed by Hshieh. As shown in Fig. 5, at the junction between a source region and a body region in a conventional device, the concentration of dopants in the body region is relatively high. This high concentration of dopants is illustrated by broken line 30 which resembles a hump. Col. 5, lines 25-27.

To flatten the concentration hump (broken line 30), Hshieh proposes to reduce the charge at the junction between a source region and the body (Xjs) by implanting dopants of the same conductivity as the source region. Thus, the concentration of dopants of the body region (which

is of opposite conductivity) is locally changed, thereby flattening the hump as seen in Fig. 4. Col. 5, lines 22-25.

Hshieh states that flattening the hump reduces the threshold voltage of the device. Col. 5, lines 30-32.

Also, Hshieh states that the local change of charge does not have an effect on the overall concentration of dopants in the body region 50. Col. 5, lines 38-43. This is illustrated by Fig. 4, which shows that the concentration of dopants at the junction of body region 50 and epitaxial layer 52 (drift region) (Xjb) is unchanged. Taking into account that Fig. 4 illustrates the concentration profile along the invertible region in body region 50 (i.e. the region that is inverted resulting in a channel between source region 48 and epitaxial layer 52), it becomes clear that Hshieh does not propose a method involving the changing of the concentration profile of the entire channel region adjacent the gate structure. That is, Hshieh can only teach the changing of only a small portion of the channel region, namely region Xjs.

Claim 11 calls for a blanket implant, i.e. "implanting dopants of a second conductivity in all of said active area of said epitaxially grown silicon layer", and then forming channel regions. The blanket implant causes variation in the dopant concentration without affecting the threshold voltage. Referring specifically to Fig. 2 of the specification, the blanket implant causes the net dopant value to be increased compared to a conventional device. See Fig. 2, line 41. The increase in the net dopant value improves the punch-through characteristics of the device. Furthermore, the blanket implant does not vary the peak dopant concentration compared to a conventional device as seen in Fig. 2. Thus, unlike the conventional method the threshold voltage remains the same.

On the other hand, Hshieh teaches a technique, which locally varies the concentration of dopants without an overall effect on the concentration in the channel, and specifically admits that its technique does not affect the punch-through characteristics of the device.

In addition, in a process according to Hshieh, the charge compensation implants are carried through a mask. Specifically, Fig.7J illustrates charge compensation implants through mask 86 after source implantation to form the source regions. Col. 7, lines 42-49. Due to the presence of the mask, there is no blanket implant. That is, there is no "implanting dopants of a

second conductivity in all of said active area of said epitaxially grown silicon layer" in that much of the active area is covered by mask 86.

Further, the blanket implant in a process according to the present invention is the same conductivity as the channel region. Thus, the net doping of the channel region is increased. See Fig. 2, line 41. Thus, claim 11 calls for the blanket implants and the channel region to be of the same conductivity (i.e. second conductivity). On the other hand, the compensation implants proposed by Hshieh are the same as the source region, and thus opposite to the channel region.

Furthermore, in Hshieh the compensation implants take place after the formation of body region 50 (see Fig. 7G) and source regions 48 (see Fig. 7I). This is clearly not the order of the process as set forth in claim 11.

Also, Hshieh does not teach the formation of multiple channel regions and a respective source region formed in each as called for by claim 11, and required for a lateral channel device. The device shown by Hshieh includes a single body region 50 in which multiple source regions 48 are formed.

In addition, Hshieh does not teach forming horizontally oriented gate structures. Rather, it teaches a trench type device with vertically oriented gate structures.

The Examiner has recognized that Hshieh fails to teach a process for forming horizontally oriented gate structures. However, the Examiner has stated that a process according to claim 11 is obvious for the following reasons:

> Kumagai, a patent from the same field of endeavor, describes in figure 3 and col. 7 lines 30 to 35 describe forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each lateral channel and in col. 11 lines 19 that vertical and horizontal devices can be interchangeable used and process steps to manufacture them are interchangeable to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in the devices, improve the speed of the device and increase current carrying capacity.
>
> Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Kumagai's teaching forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each lateral channel and of vertical and horizontal devices can be interchangeable used and process steps to manufacture them are interchangeable. In Hshieh's method

the motivation to make above substitution is to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in the devices, improve the speed of the device and increase current carrying capacity.

Further, Baliga, also, in figures 4-5 and col. 2 lines 26 to line 68 describe the interchangeable use of vertical (grooved) and horizontal (planar) semiconductor devices in power devices like FETs to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in the devices, improve the speed of the device and increase current carrying capacity.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Baliga's teaching of vertical and horizontal devices can be interchangeable used and process steps to manufacture them are interchangeable. In Hshieh's method. The motivation to make above substitution is to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in the devices, improve the speed of the device and increase current capacity. (Underlining Added).

Kumagai at col. 11, lines 1-9 states the following:

> While in the above embodiments, the explanations have been given for the semiconductor substrates based on a so-called vertical semiconductor device in which the cathode electrode and the anode electrode are formed in a relation of front surface and a rear surface, it, of course, suffices that the semiconductor may be a so-called horizontal semiconductor device with a cathode electrode and anode electrode formed on the same face as the semiconductor substrate.

Thus, Kumagai does not state that vertically oriented and horizontally oriented gate structures are interchangeable. Rather, it states that the invention it discloses applies to both a

vertical conduction device (power contacts on two opposing surfaces) or a horizontal conduction device (power contacts on the same surface). Kumagai is not referring to vertically oriented gate structures at all. Moreover, it does not state the general proposition that "vertical and horizontal devices can be interchangeable and process steps to manufacture them are interchangeable" in all contexts. Most importantly, Kumagai does not suggest a clear motivation and teaching to modify Hshieh's process to produce a device with horizontally oriented gate structures. Kumagai's statement only refers to the device it discloses, not to all devices generally.

Baliga at col. 2, lines 26-68 states:

> In the device 40 of FIG. 4, the MOS gate is formed on a surface 41 extending from the N+cathode 42 through the P-base 43 into a small portion of the N-base 44. In the device 50 of FIG. 5, the MOS gate is formed on a surface 51 extending along V-groove 52 from the N+cathode 53 through the P-base layer 54 into N-base 55. These devices will block current flow with either positive or negative voltages applied to their respective anodes 45, 56 in the absence of the gate bias. However, for positive anode voltages, the devices can be triggered into the conducting mode by application of a suitable positive voltage on the respective gates 46, 57. When a positive gate voltage is applied, the electric field across the gate oxide layers 47, 58 produces a depletion of carriers in the p-base under the gate electrode. As a result, the depletion layer in the p-base extends closer to the N+cathode region under the gate. This reduces the thickness of the undepleted p-base region of the upper NPN transistor under the gate electrode and thus increases its current gain. It is well known that a pnpn thyristor structure will switch state when the sum of the current gains of the NPN and PNP transistors, α_{NPN} and α_{PNP}, respectively, exceeds unity. In the MOS gated thyristor, resistor increases until $\alpha_{NPN} + \alpha_{PNP}$ exceeds unity. At this point strong injection of carriers must occur from the N+cathode into the p-base for the device to switch to the on-state. This requires that the N+P junction become forward biased by more that 0.5 volts. Once this takes place, the device switches to the conducting state and removal of the gate bias voltage will not cause the device to return to the blocking state because of the self-sustaining regenerative action inherent in the pnpn thyristor structure. Thus, these devices have the advantage of requiring low gate power to turn-on the thyristor via the MOS gate, but do not exhibit gate turn-off capability. Thus, the device must be returned to the blocking state by reversal of the anode polarity.

It is clear that the statements attributed to Baliga are no where to be found in the cited passage. Specifically, there is no statement in the cited passage indicating the universal concept of interchangeability of horizontal and vertical gate structures as relied on by the Examiner. Certainly, nothing has been cited to direct a skilled person in the art to modify the process shown by Hshieh to obtain a device with horizontally oriented gate structures.

It is respectfully submitted, therefore, that the record does not contain a *prima facie* case of obviousness.

VIII. CONCLUSION

Claims 11-18 are not obvious over the cited references.

If this communication is filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

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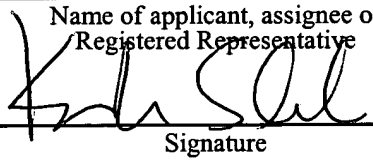

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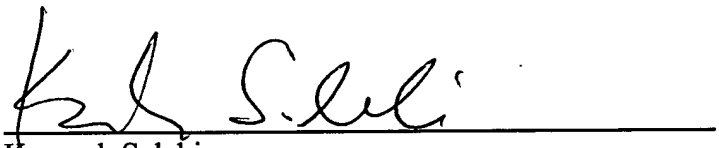
Respectfully submitted,



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CLAIMS APPENDIX

11. A process for manufacturing a planar power semiconductor device comprising:

providing a semiconductor die including an epitaxially grown silicon layer of a first conductivity formed over a substrate;

designating an active area, said active area being a portion of said epitaxially grown silicon layer in which channel regions are formed;

implanting dopants of a second conductivity in all of said active area of said epitaxially grown silicon layer;

forming a plurality of spaced channel regions of said second conductivity in said active area of said epitaxially grown silicon layer, each channel region being spaced from another channel region by a first conductivity region in said epitaxially grown silicon layer;

forming a source region of said first conductivity in each of said channel regions, each source region being less wide and less deep than a channel region in which it is formed; and

forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each channel region.

12. A process according to claim 11, further comprising forming a field oxide termination structure at the edge of said active area prior to said implanting step.

13. A process according to claim 11, further comprising forming a field oxide termination structure at the edge of said active area after said implanting step.

14. A process according to claim 11, wherein said gate structure comprises a gate oxide, said gate oxide being formed after said implanting step.

15. A process according to claim 12, wherein said field oxide is formed over said epitaxially grown silicon and etched to provide a window over said active area, wherein said dopants of said second conductivity are implanted through said window.

16. A process according to claim 11, wherein said dopants of said second conductivity are comprised of boron.

17. A process according to claim 11, wherein said dopants of said second conductivity type are comprised of either arsenic or phosphorous.

18. A process according to claim 11, further comprising, forming an oxide interlayer over said gate structure; opening windows in said oxide interlayer over at least said source regions; and forming a source contact over said oxide interlayer and a heavy base region.